What is claimed is:

1.   A method comprising configuring a plurality of processing elements within a heterogeneous configurable circuit to demultiplex a data stream, operate on portions of the data stream in parallel, and multiplex results to a second data stream.

2.   The method of claim 1 wherein configuring a plurality of processing elements comprises configuring a plurality of processing elements capable of filtering data.

3.   The method of claim 2 wherein configuring a plurality of processing elements further comprises configuring at least one programmable element to demultiplex the data stream into non-overlapping segments.

4.   The method of claim 3 wherein the non-overlapping segments comprise data packets.

5.   The method of claim 4 wherein configuring at least one programmable element comprises configuring the at least one programmable element to route data packets to a plurality of processing elements capable of filtering data.

6.   The method of claim 1 wherein configuring a plurality of processing elements further comprises configuring at least one programmable element to demultiplex the data stream into overlapping segments.

7.   The method of claim 6 wherein the overlapping segments comprise data packets.

3   8.   The method of claim 7 wherein configuring at least one programmable

4   element comprises configuring the at least one programmable element to route data

5   packets to a plurality of processing elements capable of filtering data.

1   9.   A method comprising configuring a heterogeneous configurable device to:

2   demultiplex a packet-based input data stream into a plurality of separate data

3   streams;

4   route the plurality of separate data streams to processing elements in

5   parallel; and

6   multiplex output packets from processing elements in parallel to produce a

7   packet-based output data stream.

1   10.   The method of claim 9 wherein configuring the heterogeneous configurable

2   device to demultiplex a packet-based input stream comprises configuring a

3   programmable element that is coupled to routers in a row and column arrangement.

1   11.   The method of claim 9 wherein configuring the heterogeneous configurable

2   device to route the plurality of separate data streams comprises configuring a

3   programmable element that is coupled to routers in a row and column arrangement.

1   12.   The method of claim 9 wherein configuring the heterogeneous configurable

2   device to multiplex output packets from processing elements in parallel comprises

3   configuring a programmable element that is coupled to routers in a row and column

4   arrangement.

1   13.   The method of claim 9 wherein configuring the heterogeneous configurable

2   device to route the plurality of separate data streams comprises configuring a

3   programmable element to route the separate data streams to a plurality of processing

4   elements capable of filtering data.

1   14.   The method of claim 13 wherein filtering data comprises performing a Fast

2   Fourier Transform.

1   15.   The method of claim 13 wherein filtering data comprises performing a finite

2   impulse response filter.

1   16.   The method of claim 9 wherein configuring the heterogeneous configurable

2   device to route the plurality of separate data streams comprises configuring a

3   programmable element to route the separate data streams to a plurality of processing

4   elements capable of implementing a Viterbi decoder.

1   17.   An apparatus including a medium to hold machine-accessible instructions

2   that when accessed result in a machine performing:

3   configuring a plurality of processing elements within a heterogeneous

4   configurable circuit to demultiplex a data stream, operate on portions of the data

5   stream in parallel, and multiplex results to a second data stream.

1   18.   The apparatus of claim 17 wherein configuring a plurality of processing

2   elements comprises configuring a plurality of processing elements capable of

3   filtering data.

1   19.   The apparatus of claim 18 wherein configuring a plurality of processing

2   elements further comprises configuring at least one router to route data packets

3   within the integrated circuit.

1   20.   An apparatus comprising:

2   a heterogeneous plurality of configurable processing elements; and

3   a plurality of interconnected routers to route packets between the plurality of

4   configurable processing elements;

5   wherein a subset of the plurality of configurable processing elements are

6   configurable to be operated in parallel.

1   21.   The apparatus of claim 20 wherein the plurality of interconnected routers are

2   configurable to demultiplex a data stream to produce a plurality of sub-streams.

1   22.   The apparatus of claim 21 wherein the plurality of interconnected routers are

2   further configurable to route the plurality of sub-streams to the subset of the

3   plurality of configurable processing elements.

1   23.   The apparatus of claim 20 wherein at least one of the plurality of

2   configurable processing elements is configurable to demultiplex a data stream to

3   produce a plurality of sub-streams.

1   24.   The apparatus of claim 23 wherein the at least one of the plurality of

2   configurable processing elements are further configurable to route the plurality of

3   sub-streams to the subset of the plurality of configurable processing elements.

1   25.   The apparatus of claim 20 wherein the subset of the plurality of configurable

2   processing elements comprises micro-coded processing elements.

1   26.   The apparatus of claim 25 wherein the micro-coded processing elements

2   comprise filter micro-coded accelerators.

1   27.   An electronic system comprising:

2   an antenna;

3   a radio frequency circuit to receive communications signals from the

4   antenna; and

5   a configurable circuit coupled to the radio frequency circuit, the configurable

6   circuit including a heterogeneous plurality of configurable processing elements, and

7   a plurality of interconnected routers to route packets between the plurality of

8   configurable processing elements, wherein a subset of the plurality of configurable

9   processing elements are configurable to be operated in parallel.

1   28.   The electronic system of claim 27 wherein at least one of the plurality of

2   configurable processing elements are configurable to demultiplex a data stream to

3   produce a plurality of sub-streams.

1   29.   The electronic system of claim 27 wherein the subset of the plurality of

2   configurable processing elements are configurable to perform a Fast Fourier

3   Transform.

1   30.   The electronic system of claim 27 wherein the subset of the plurality of

2   configurable processing elements are configurable to perform a finite impulse

3   response filter.